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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/582,833	06/14/2006	Ari Pekkarinen	915-001.090	6761

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EXAMINER	
YEUNG LOPEZ, FEIFEI	
ART UNIT	PAPER NUMBER
2826	
MAIL DATE	DELIVERY MODE
06/13/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,833	PEKKARINEN ET AL.	
	Examiner	Art Unit	
	FEI FEI YEUNG LOPEZ	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/14/06; 07/26/07;6/2/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Amendments to the claims and the specification are acknowledged and entered. Applicants argue that the species shown in figs. 1-3 have a list of common features and therefore restriction is improper. According to the MPEP, restriction is proper when inventions are "independent or distinct as claimed" and when there is serious burden to search (see MPEP 803). Though there are some common elements in figs. 1-3, they are distinct from each other at least by having different configurations of electroconductive elements. However, as the way the claimed are written now, there is no serious burden to search. Therefore, all claims are examined. On the other hand, Applicants have elected species I and shall not add limitations to the claims non-elected features until petition to overturn the restriction requirement is granted.

Claim Objections

2. Claims 5-7, 12-14, and 20 are objected to because of the following informalities: "[T]he cover element" lack antecedent basis and should be "the cover element". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-5, 8-9, 11-12, 15-17, and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Thomason et al (US Patent 6,421,221 B1).

5. Regarding claim 1, Thomason teach a semiconductor component, comprising a semiconductor element and an electroconductive element (element 18 in fig. 2) comprising at least one outlet, wherein the at least one outlet is configured to connect the electroconductive element to ground in order to shield the semiconductor element against electrostatic pulses (column 3, lines 5-11).

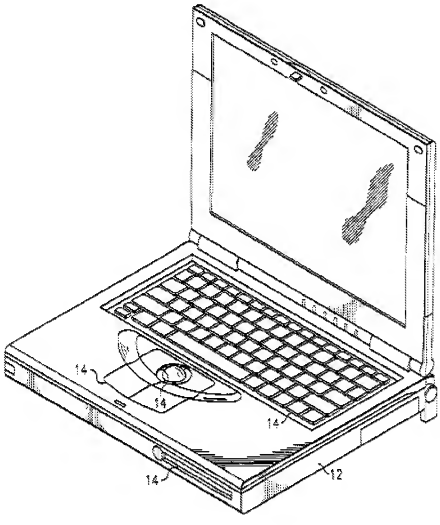

Fig. 1

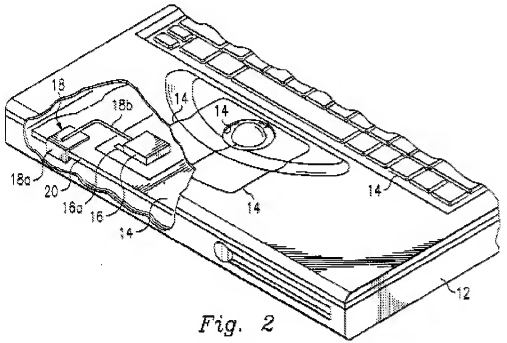

Fig. 2

6. Regarding claim 2, Thomason teach a semiconductor component according to claim 1, wherein in structure, the electroconductive element is a planar sheet (element 18 in fig. 2).

7. Regarding claim 4, Thomason teach a semiconductor component according to claim 1, wherein the electroconductive element forms a permanent, integrated part of the semiconductor component (see figs. 1 and 2).

8. Regarding claim 5, Thomason teach a semiconductor component according to claim 4, wherein the electroconductive element is placed underneath a cover element (layer 12 in fig. 2) of the semiconductor component, inside said cover element.

9. Regarding claim 8, Thomason teach a method for shielding a semiconductor element against electrostatic pulses, comprising: integrating the semiconductor element in a semiconductor component, integrating an electroconductive element (element 18 in fig. 2) in the semiconductor component and providing at least one outlet for the integrated electroconductive element, so that the at least one outlet is configured to connect the electroconductive element to ground (column 3, lines 5-11).

10. Regarding claim 9, Thomason teach a method according to claim 8, wherein in the semiconductor component, there is integrated an electroconductive, planar element (element 18 in fig. 2).

11. Regarding claim 11, Thomason teach a method according to claim 8, wherein the electroconductive element is integrated as a permanent part of the semiconductor component (figs. 1 and 2).

12. Regarding claim 12, Thomason teach a method according to claim 11, wherein the electroconductive element is integrated underneath a cover element (layer 12 in fig. 2) of the semiconductor component, inside said cover element.

13. Regarding claim 15, Thomason teach an arrangement including a mounting tray (layer 12 in fig. 2) and at least one semiconductor component, wherein said at least one semiconductor component comprises a semiconductor element and an integrated electroconductive element (element 18 in fig. 2), where the electroconductive element is provided with at least one outlet that is grounded (column 3, lines 5-11) to a ground plane of the mounting tray.

14. Regarding claim 16, Thomason teach an apparatus for shielding a semiconductor element against electrostatic pulses, comprising: means for integrating the semiconductor element in a semiconductor component; and means for integrating an electroconductive element (element 18 in fig. 2) in the semiconductor component and for providing at least one outlet for the integrated electroconductive element, so that the at least one outlet is configured to connect the electroconductive element to ground (column 3, lines 5-11).

15. Regarding claim 17, Thomason teach the apparatus of claim 16, wherein in the semiconductor component, there is integrated an electroconductive, planar element (element 18 in fig. 2).

16. Regarding claim 19, Thomason teach the apparatus of claim 16, wherein the electroconductive element is integrated as a permanent part of the semiconductor component (see figs. 1 and 2).

17. Regarding claim 20, Thomason teach the apparatus of claim 16, wherein the electroconductive element is integrated underneath a cover element (layer 12 in fig. 2) of the semiconductor component, inside said cover element.

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Initially, and with respect to claims 1,8, and 16, note that a limitation in a claim with respect to the manner in which a claimed device is intended to be used does not differentiate the claimed device from a prior-art device if the prior-art device teaches all structural limitations in the claims and the functional limitations are found to be inherent in the prior art device. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See *Hewlett-Packard Co. v. Bausch & Lomb Inc.* and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a device claim, and not the patentability of its functions (909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990)). As stated in Best, Where the claimed and prior art products are identical or substantially identical in structure or composition, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). Note that the applicant has burden of proof once the examiner establishes a sound basis for believing that the products of the applicant and the prior art are the same. See *In re Spada*, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990).

19. Claims 1,3,8,10,16, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Whitney et al (PG Pub 2004/0035598 A1).

20. Regarding claim 1, Whitney teach a semiconductor component, comprising a semiconductor element and an electroconductive element (layer 30 in fig. 2) comprising at least one outlet, wherein the at least one outlet is configured to connect the electroconductive element to ground (paragraph [0009]). Note that "to shield the

semiconductor component element against electrostatic pulses" is functional language that does not carry patentable weight since Whitney teach all structural elements of the claim.

21. Regarding claim 3, Whitney teach a semiconductor component according to claim 1, wherein the electroconductive element is a thin loop structure (see fig. 5)

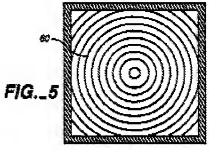

FIG._5

22. Regarding claim 8, Whitney teach a method comprising: integrating the semiconductor element in a semiconductor component, integrating an electroconductive element (layer 30 in fig. 2) in the semiconductor component and providing at least one outlet for the integrated electroconductive element, so that the at least one outlet is configured to connect the electroconductive element to ground (paragraph [0009]). Note that "a method for shielding a semiconductor element against electrostatic pulses" is functional language that does not carry patentable weight since Whitney teach all structural elements of the claim.

23. Regarding claim 10, Whitney teach a method according to claim 8, wherein in the semiconductor component, there is integrated an electroconductive, loop-shaped element (fig. 5).

24. Regarding claim 16, Whitney teach an apparatus for shielding a semiconductor element against electrostatic pulses, comprising: means for integrating the semiconductor element in a semiconductor component; and means for integrating an electroconductive element (layer 30 in fig. 2) in the semiconductor component and for providing at least one outlet for the integrated electroconductive element, so that the at least one outlet is configured to connect the electroconductive element to ground (paragraph [0009]).

25. Regarding claim 18, Whitney teach the apparatus of claim 16, wherein in the semiconductor component, there is integrated an electroconductive, loop-shaped element (fig. 5).

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

28. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomason et al (US Patent 6,421,221 B1) as applied to claims 4 and 11 above, and further in view of Awujoola et al (PG Pub 2005/0104164 A1).

29. Regarding claim 6, Thomason remain as applied in claim 4. However, Thomason do not teach that the electroconductive element is placed on top of a cover element of the semiconductor component, outside said cover element. In the same field of endeavor, Awujoola teach an electroconductive element (layer 110 in fig. 2) is placed on top of a cover element (layer 170) of the semiconductor component, outside said cover element for the benefit of providing an EMI protection (abstract). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include an electroconductive element placed on top of a cover element of the semiconductor component, outside said cover element for the benefit of providing an EMI protection.

30. Regarding claim 13, Thomason remain as applied in claim 11. However, Thomason do not teach that the electroconductive element is integrated on top of a cover element of the semiconductor component, outside said cover element. In the same field of endeavor, Awujoola teach an electroconductive element (layer 110 in fig. 2) is integrated on top of a cover element (layer 170) of the semiconductor component, outside said cover element for the benefit of providing an EMI protection (abstract). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include an electroconductive element integrated on top of a cover element

of the semiconductor component, outside said cover element for the benefit of providing an EMI protection.

31. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomason et al (US Patent 6,421,221 B1) as applied to claim1 above, and further in view of Sasaki et al (PG Pub 2004/0257700 A1).

32. Regarding claim 7, Thomason remain as applied in claim 1. However, Thomason do not teach that the electroconductive element is induced in the cover element of the semiconductor component either chemically or electrochemically. In the same field of endeavor, Sasaki teach an electroconductive element is induced chemically (CVD ,see paragraph [0097]) for the benefit of providing good step coverage. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to induce the electroconductive element chemically for the benefit of providing good step coverage.

33. Regarding claim 14, Thomason remain as applied in claim 11. However, Thomason do not teach that the electroconductive element is induced in the cover element of the semiconductor component either chemically or electrochemically. In the same field of endeavor, Sasaki teach an electroconductive element is induced chemically (CVD, see paragraph [0097]) for the benefit of providing good step coverage. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to induce the electroconductive element chemically for the benefit of providing good step coverage.

34. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitney et al (PG Pub 2004/0035598 A1) as applied to claim1 above, and further in view of Sasaki et al (PG Pub 2004/0257700 A1).

35. Regarding claim 7, Whitney remain as applied in claim 1. However, Whitney do not teach that the electroconductive element is induced in the cover element of the semiconductor component either chemically or electrochemically. In the same field of endeavor, Sasaki teach an electroconductive element is induced chemically (CVD ,see paragraph [0097]) for the benefit of providing good step coverage. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to induce the electroconductive element chemically for the benefit of providing good step coverage.

36. Regarding claim 14, Whitney remain as applied in claim 11. However, Whitney do not teach that the electroconductive element is induced in the cover element of the semiconductor component either chemically or electrochemically. In the same field of endeavor, Sasaki teach an electroconductive element is induced chemically (CVD, see paragraph [0097]) for the benefit of providing good step coverage. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to induce the electroconductive element chemically for the benefit of providing good step coverage.

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is (571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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